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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,375	10/16/2001	Yoshinobu Ono	2185-0578P	3053
2292	7590	07/18/2002	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			IM, JUNGHWA M	
		ART UNIT	PAPER NUMBER	
		2811		
DATE MAILED: 07/18/2002				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/977,375	ONO ET AL.
	Examiner	Art Unit
	Junghwa M. Im	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 20 June 2002.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) 12, 13 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-11 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 .	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-11 in Paper No. 9 is acknowledged.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 recites a fragment of a sentence and does not carry an explicit meaning.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3, 6, and 7 are rejected under 35 U.S.C. 103 (a) as being unpatentable

over Mishima et al. (U.S. Pat. No. 5,633,516) in view of Inoue (U.S. Pat. No. 5,134,446) and Kizuki (U.S. Pat. No. 5,948,161).

Regarding claim 1, Mishima et al. show, in Fig. 1, a 3-5 group compound semiconductor comprising

a GaAs substrate (1), a buffer layer (2) on said GaAs substrate and an epitaxial crystal layer (5) on said buffer layer, and said layers being formed by an epitaxial crystal growth method, wherein said buffer layer and said epitaxial crystal layer on said buffer layer are 3-5 group compound semiconductors each independently represented by the general formula $\text{In}_x\text{Ga}_y\text{Al}_z\text{As}$ (wherein, $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$, $x + y + z = 1$) (col. 3, lines 26-52 and col. 4, lines 28-34).

Mishima et al. do not explicitly show that the dislocation density in the epitaxial crystal layer on the buffer layer is $2000/\text{cm}^2$ or less.

Inoue teaches that a semiconductor device of GaAs substrate with a buffer structure having the dislocation density of the crystal layers (13, 15 in Fig. 2) with the limitation of the claimed invention as recited above (col. 5, lines 8-18).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Inoue into the device taught by Mishima et al. since the device breakdown can be alleviated through the reduction of the defect density and resulting lattice-misfit.

Kizuki also motivates a defect density of less than $2000/\text{cm}^2$ at column 11, lines 2-12.

Such a defect density would have been obvious in order to have a high quality device layer as taught by Kizuki.

Regarding claim 2, Mishima et al. disclose most aspects of the claimed invention as discussed in claim1.

Mishima et al. do not show that the dislocation density in the epitaxial crystal layer on the buffer layer is 1/3 or less of the dislocation density in said GaAs substrate.

Inoue, however, shows that the dislocation density of the crystal layer on the buffer layer is 1/3 or less of the dislocation density of the substrate through following example.

In col.1, lines 44-48, Inoue discloses the GaAs substrate with a dislocation density of $10^{12} /cm^2$. And Inoue discloses, in col. 5, lines 8-18, the dislocation density of the crystal layer on the buffer layer can be reduced to about $1x 10^6/cm^2$.

Regarding claim 3, Mishima et al. disclose that the 3-5 group compound semiconductor the said buffer layer has a structure formed by laminating at least two kinds of layers having different compositions, for n ($1 \leq n \leq 30$) times (col.3, lines 26-52, col.4, lines 28-34).

Regarding claim 6, Mishima et al. show that at least one layer of two kinds of layers in the buffer layer is doped with an n-type dopant (col. 5, line 22 and col.4, lines 28-34).

Regarding claim 7, Mishima et al. show that said n-type dopant is Si and the concentration of the Si is $1x 10^{17} cm^{-3}$ or less (col.5, lines 43-45).

5. Claims 4, 5 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mishima et al. and Inoue as applied to claims 1-3 above, and further in view of Schmitz et al. (U.S. Pat. No. 6,316,820).

Regarding claim 4, Mishima et al. and Inoue do not disclose that two kind of layers in the buffer layer are a $\text{Ga}_{1-z}\text{Al}_z\text{As}$ layer (wherein, $0 < z \leq 1$) and a GaAs layer.

Schmitz et al. show that a device with a buffer layer (26) in Fig.1 made of AlGaAs/GaAs.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Schmitz et al. into the device taught by Mishima et al. and Inoue since the heterojunction structure of the buffer layer absorbs the dislocation gradually and improves the performance of the device.

Regarding claim 5, Inoue teaches that the value of z in one of the buffer layers ($\text{Ga}_{1-z}\text{Al}_z\text{As}$ layer) can be 0.1 or more and 0.4 or less. Although the buffer layer of Inoue is made of $\text{Ga}_{1-z}\text{In}_z\text{As}$, it is also taught that In can be replaced with other group III elements, such as B or Al (Col.7, lines 20-23). Further, Inoue discloses that the composition of the In content is not limited and can be smaller or larger (col.6, line 55 – col.7, line 6).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to choose relative composition of the element as recited in the claim, in order to achieve maximum absorption of the distortion cause as a result of the lattice mismatch.

Regarding claims 8 –10, Mishima et al. show that the buffer layer is doped with n

type Si dopant as discussed above.

Schmitz et al. disclose that Si planar dopant layer on the upper portion of the buffer layer which is recited in the instant claim as "on the interface of at least one layer of two kinds of layers " (col.5, lines 61-65).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Schmitz et al. into the device taught by Mishima et al. and Inoue since propagation of the distortion toward the upper layer is suppressed through uniform doping on a specific plane in a buffer layer, resulting in improved reliability of the device.

Regarding the planar doping concentration, Mishima et al. teach the concentration of Si in terms of volume as discussed above, while the instant claim recites the identical concentration range in term of surface area.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Art Unit: 2811

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JMI

July 12, 2002

Sara W Crane
Sara Crane
Primary Examiner